Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A thyristor structure, comprising:

a first terminal formed as a first region having a first conductivity type;

a second region of a second conductivity type adjoining said first region;

a third region of the first conductivity type adjoining said second region and having a common surface with said second region;

a second terminal functioning as a fourth region, formed of the second conductivity type, and adjoining said third region;

auxiliary electrodes disposed on said common surface and each adjoining one of said second and third regions, said auxiliary electrodes being formed as gate electrodes and being

electrically conductively connected with a respective one of said first terminal and said second terminal; and

a control terminal for controlling the thryistor structure by an applied current embodied in one of said second region and said third region.

Claim 2 (original). The thyristor structure according to claim 1, wherein said auxiliary electrodes are each formed from a conductive region made of polysilicon and an auxiliary oxide insulating said conductive region from said common surface.

Claim 3 (currently amended). An overvoltage protection configuration, comprising:

a thyristor structure containing:

a first terminal formed as a first region having a first conductivity type;

a second region of a second conductivity type adjoining said first region;

a third region of the first conductivity type adjoining said second region and having a common surface with said second region;

a second terminal functioning as a fourth region, formed of the second conductivity type, a component to be protected disposed in an electrically conductive manner between said first terminal and said second terminal;

auxiliary electrodes disposed on said common surface and each adjoining one of said second and third regions, said auxiliary electrodes being formed as gate electrodes and being electrically conductively connected with a respective one of said first terminal and said second terminal; and

a control terminal for controlling the thryistor structure by an applied current embodied in one of said second region and said third region; and

an overvoltage detector connected to and detecting an overvoltage across the component to be protected.

Claim 4 (original). The overvoltage protection configuration according to claim 3, wherein said control terminal forms a

fifth region and is formed of the first conductivity type, said fifth region having a higher conductivity than said third region.

Claim 5 (original). The overvoltage protection configuration according to claim 3, wherein a supply voltage of the component to be protected is connected to said first terminal and to said second terminal.

Claim 6 (currently amended). An overvoltage protection configuration, comprising:

a single semiconductor chip;

a thyristor structure integrated in said single semiconductor chip and containing:

a first terminal formed as a first region having a first conductivity type;

a second region of a second conductivity type adjoining said first region;

a third region of the first conductivity type adjoining said second region and having a common surface with said second region;

a second terminal functioning as a fourth region, formed of the second conductivity type, a component to be protected disposed in an electrically conductive manner between said first terminal and said second terminal;

auxiliary electrodes disposed on said common surface and each adjoining one of said second and third regions, said auxiliary electrodes being formed as gate electrodes and being electrically conductively connected with a respective one of said first terminal and said second terminal;

a control terminal for controlling the thryistor structure by an applied current embodied in one of said second region and said third region; and

an overvoltage detector connected to and detecting an overvoltage across the component to be protected.